CLAIMS:

What is claimed is:

1. A signal recovery method for a self-clocked transmission system, comprising the steps of:

inputting a received data signal to both a first monostable circuit component and a second monostable circuit component;

generating a first output signal from the first monostable circuit component and a second output signal from the second monostable circuit component;

comparing the first output signal and the second output signal to each other using a first logical operator; and

outputting a compared output signal based on the comparison.

2. The method of claim 1, wherein the signal recovery consists of at least one of a clock signal and a data signal.

3. The method of claim 1, wherein the received data signal is at least one of a processed equalized data signal and a processed unequalized data signal.

4. The method of claim 1, wherein the first logical operator is an OR-gate logical operator.

5. The method of claim 1, wherein the compared output signal is a recovered clock output signal.

6. The method of claim 5, wherein the recovered clock output signal is at least one of a positive edge clock

signal and a negative edge clock signal.

7. The method of claim 1, wherein at least one of the first monostable circuit component and the second monostable circuit component are one-shot circuit components.

8. The method of claim 1, wherein the first generated output signal is at least one of a ones clock output signal and a zeros clock output signal.

9. The method of claim 1, wherein the second generated output signal is at least one of a ones clock output signal and a zeros clock output signal.

10. The method of claim 3, wherein equalizing the inputted data signal includes;

differentiating the inputted data signal;

amplifying the differentiated data signal;

applying a sign element to the amplified data signal; and

decreasing the signed amplified data signal.

11. The method of claim 10, further comprising:

combining a constant value with the signed amplified data signal.

12. The method of claim 10, wherein differentiating the received data signal includes a resistive-capacitive differentiator.

13. The method of claim 3, wherein processing the data signal comprises:

integrating the equalized data signal;

generating a third output signal, wherein the integrated equalized data signal is compared to a peak threshold within a relational operator;

inputting the third generated output signal to a first flip-flop circuit device; and

outputting a fourth output signal from the first flip-flop circuit component.

14. The method of claim 13, wherein the third generated output signal is at least one of a mid-bit zero output signal and a mid-bit one output signal.

15. The method of claim 13, wherein the equalized data signal uses a resistive-capacitive integrator.

16. The method of claim 13, wherein comparing the integrated equalized data signal within the relational operator is at least one of a greater than relational operator and a less than relational operator.

17. The method of claim 13, wherein the peak threshold is at least one of a positive peak threshold and a negative peak threshold.

18. The method of claim 13, wherein the first flip-flop circuit component is a set-reset flip-flop circuit component.

19. The method of claim 13, wherein inputting the third generated output signal to the first flip-flop circuit component is inputted to at least one of a set input

terminal and a reset input terminal.

20. The method of claim 13, wherein the fourth generated output signal is at least one of an asynchronous recovered non-return to zero output signal and a complementary recovered non-return to zero output signal.

21. The method of claim 13, wherein processing the inputted equalized data signal further includes:

inputting the third generated output signal to a second logical operator; and

outputting a fifth output signal from the second logical operator, wherein the fifth output signal is a mid-bit output signal.

22. The method of claim 21, wherein the second logical operator is an OR-gate logical operator.

23. The method of claim 1, wherein inputting the data signal to both a first monostable circuit component and a second monostable circuit component further includes:

inputting a processed equalized data signal to the first monostable circuit component;

inputting an asynchronous recovered non-return to zero output signal to the first monostable circuit component; and

inputting a processed equalized data signal to the second monostable circuit component; and

inputting an complementary asynchronous recovered non-return to zero output signal to the second monostable circuit component.

24. The method of claim 23, wherein inputting a processed

equalized data signal to the first monostable circuit component is inputted at a trigger input terminal.

25. The method of claim 23, wherein inputting the asynchronous recovered non-return to zero output signal to the first monostable circuit component is inputted to an enable input terminal.

26. The method of claim 23, wherein inputting a processed equalized data signal to the second monostable circuit component is inputted to a trigger input terminal.

27. The method of claim 23, wherein inputting the complementary asynchronous recovered non-return to zero signal to the second monostable circuit component is inputted to an enable input terminal.

28. The method of claim 1, wherein the compared output signal is a clock output signal.

29. The method of claim 1, further comprising:

inputting the compared output signal at a second flip-flop circuit component;

inputting an asynchronous recovered non-return to zero output signal at the second flip-flop circuit component;

inputting a constant signal at the second flip-flop circuit component; and

outputting a synchronous recovered non return to zero output signal from the second flip-flop circuit component based on at least one of the compared output signal, the asynchronous recovered non-return to zero output signal, and the constant signal inputs.

30. The method of claim 29, wherein the second flip-flop circuit component is a data flip-flop circuit component.

31. The method of claim 29, wherein inputting the compared output signal at the second flip-flop circuit component is inputted at a clock input terminal.

32. The method of claim 29, wherein inputting the asynchronous recovered non-return to zero output signal at the second flip-flop circuit component is inputted at a data input terminal.

33. The method of claim 29, wherein inputting the constant signal at the second flip-flop circuit component is inputted at a complementary clock input terminal.

34. The method of claim 29, wherein the output signal is outputted from the second flip-flop circuit component from at least one of an output terminal and a complementary output terminal.

35. A signal recovery system for a self-clocked transmission system, comprising:

an equalizer, wherein the equalizer has at least one output port;

a first monostable circuit component having at least two input ports and two output ports, wherein the output port of the equalizer is connected to a first input port of the first monostable circuit component;

a second monostable circuit component having at least two input ports and two output ports, wherein the output of

the equalizer is connected to a first input port of the second monostable circuit component; and

a first logical operator having at least two input ports and one output port, wherein a first output port of the first monostable circuit component is connected to a first input port of the first logical operator and a first output port of the second monostable circuit component is connected to the second input port of the first logical operator.

36. The system of claim 35, further comprising:

a data flip-flop circuit component having a data input port, a clock input port and a complementary clock input port and having an output port and a complementary output port, wherein the output port of the first logical operator is connected to the clock input port of the data flip-flop circuit component; and

a constant signal source, wherein the constant signal source is connected to the complementary clock input port of the data flip-flop circuit component.

37. The system of claim 35, wherein the first logical operator is an OR-gate.

38. The system of claim 35, wherein both the first monostable circuit component and the second monostable circuit component are both one-shot circuit components having at least two input ports and two output ports, and wherein the first input port on both the one-shot circuit components is an enable input port and the second input port is a trigger input port and the first output port on both one-shot circuit components is a positive edge output port

and the second output port is a negative edge output port.

39. The system of claim 35, further comprising:

an integrator having at least one input port and one output port, wherein the output port of the equalizer is connected to the input port of the integrator;

a first relational operator having at least two input ports and one output port, wherein the output of the integrator is connected to a first input port of the first relational operator and a threshold constant signal source is connected to a second input port of the first relational operator; and

a second relational operator having at least two input ports and one output port, wherein the output of the integrator is connected to a first input port of the second relational operator and a threshold constant signal source is connected to a second input port of the second relational operator.

40. The system of claim 39, wherein the equalized data signal uses a resistive-capacitive integrator.

41. The system of claim 39, wherein the first relational operator is a greater than relational operator.

42. The system of claim 39, wherein the second relational operator is a less than relational operator.

43. The system of claim 39, wherein the threshold constant signal source is at least one of a positive peak threshold source and a negative peak threshold source.

44. The system of claim 39, further comprising:

a second logical operator having at least two input ports, wherein the output of the first relational operator is connected to a first input port of the second logical operator and the output of the second relational operator is connected to a second input port of the second logical operator.

45. The system of claim 44, wherein the second logical operator is an OR-gate.

46. The system of claim 39, further comprising:

a set-reset flip-flop circuit component, wherein the set-reset flip-flop circuit component has a set input port and a reset input port and has an output port and a complementary output port, wherein the output of the first relational operator is connected to the reset input port of the set-reset flip-flop circuit component and the output of the second relational operator is connected to the set input port of the set-reset flip-flop circuit component, the output port of the set-reset flip-flop circuit component is connected to the enable input port of the first monostable circuit component and the complementary output port of the set-reset flip-flop circuit component is connected to the enable input port of the second monostable circuit component, and wherein the output port is further connected to the data input of the data flip-flop circuit component.

47. A signal recovery circuit for a self-clocked transmission system, comprising:

an equalizing circuit having a signal input for receiving a data signal and a signal output for outputting

an equalized data signal;

a first monostable clock edge sensing circuit having a trigger signal input connected to the output of the equalizing circuit, an enable input, a positive edge output, and a negative edge output;

a second monostable clock edge sensing circuit having a trigger input connected to the output of the equalizing circuit, an enable input, a positive edge output, and a negative edge output; and

a first logical operator having one input connected to the positive edge output of the first monostable positive clock edge sensing circuit and a second output connected to the second monostable negative clock edge sensing circuit and a signal output for outputting a recovered clock out signal.

48. The circuit in claim 47, further comprising:

an integrating circuit having a signal input connected to the equalized data signal and a signal output for outputting an equalized integrated data signal;

a relational circuit having a first relational operator element connected at a first input to the output of the integrating circuit and a second input connected to a first peak threshold element and a second relational operator element having a first input connected to the output of the integrating circuit and a second input connected to a second peak threshold element; and

a first flip-flop circuit having a set input connected to an output of the second relational operator element and a reset input connected to an output of the first relational operator element, an output connected to the enable input of the first monostable clock edge sensing circuit, and a

complementary output connected to the enable input of the second monostable clock edge sensing circuit.

49. The circuit in claim 47, further comprising:

a second logical element connected at one input to the output of the first relational operator element output and a second input connected to the output of the second relational operator element.

50. The circuit in claim 47, further comprising:

a second flip-flop circuit having a data input connected to the output of the first logical circuit element, having a clock input connected to the output of the first flip-flop circuit, and a complementary clock input connected to a constant signal.